

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re application of:

Chidambarao Dureseti, *et. al.*

Group Art Unit: 2814

Serial No.: 10/605,108 yet

Examiner: Pham, Long

Filed: September 9, 2003

**For: METHOD FOR REDUCED N+ DIFFUSION IN STRAINED SI ON SIGE
SUBSTRATE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.56**

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the cited documents is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that these documents be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in payment and credit any overpayments to International Business Machines Corporation's deposit account no. 09-0458.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Andrew M. Calderon".

Andrew M. Calderon
Reg. No. 38,093

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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENTApplicant:
Dureseti Chidambarao, et al.

(Use several sheets if necessary)

Page 1 of 1

Filing Date:
September 9, 2003Group:
2814

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
		Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
		F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
		Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
		K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.